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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/078,276	02/20/2002	William Henry Oldfield	550-317	3420

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EXAMINER

COLEMAN, ERIC

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/078,276	Applicant(s) OLDFIELD ET AL.	
	Examiner Eric Coleman	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 February 2002 and 07 May 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3,8 and 12-14 is/are rejected.
- 7) ☒ Claim(s) 4-7 and 9-11 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3,8,12-14 rejected under 35 U.S.C. 103(a) as being unpatentable over by Trivedi (patent No. 6,430,674).

3. Trivedi taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Processor core (304) for executing instructions for any of a plurality of instruction sets (e.g., see fig.3 and col. 2, lines 35-60 and col.5, line14- col. 6, line 28);
and

b) Prediction logic for predicting which instructions should be retrieved from memory and to review retrieved instruction to predict whether the execution of that retrieved instruction will cause a change in instruction flow, and if so to indicate to the retrieval means an address within the memory from which a next instruction should be retrieved and whether the retrieved instruction would additionally cause a change in instruction set, and if so to cause an instruction set identification signal to be generated for sending to the processor core to indicate the instruction set to which the next

Art Unit: 2183

instruction belongs (e.g., see col. 8, lines 35-58 and col. 6, line 29-col. 7, line 50, and col. 3, lines 34-62).

4. Trivedi did not expressly detail (claim 1,13,14) a prefetch unit for prefetching instructions prior to sending those to the processor core. Trivedi, however, taught a memory (102) mass storage device (103) external to processor (104) (e.g., see fig. 1) and instruction cache within processor (104) for storing instructions for execution and a fetch unit (302a) within the processor. Trevedi also taught the advantage of fetching early because the first fetch usually incurs a cache miss (e.g., see col. 7, lines 51-59) A cache conventionally comprises a fast small memory where instruction and/or data are fetched from slow larger external storage so that the latency for access to instructions and/or data is reduced. Therefore one of ordinary skill would have been motivated to incorporate a prefetch unit to provide instructions from the external memory at least to take advantage of the access speed of the cache for providing instructions for execution and reduce latency of retrieval or instructions.

5. As per claim 2, Trevedi taught prediction logic arranged to detect the presence of an instruction of a first type which when executed will cause a change in instruction set if execution also results in the change in instruction flow (e.g., see col. 6, lines 29-63 and col. 8, lines 35-58).

6. As per claim 3, Trevedi taught branch instructions that if committed changed the change in instruction flow, which indicates that the when committed the change would have been for at least some of the branch instructions unconditional (e.g., see col. 8, lines 35-58).

Art Unit: 2183

7. As per claims 8, Trevedi taught prediction logic that comprised branch prediction logic and the change in instruction flow results from execution of a branch instruction (e.g., see col. 8, lines 35-58).

8. As per claim 12, Since the predictions in the Trevedi system provided predictions for wake-up of system components dependent on the prediction outcome of instructions to be stored in the cache, one of ordinary skill would have been motivated to provide the prediction logic within the portion of the system that performed the fetching of instructions from memory to cache to make the prediction as early as possible so the wake-up could be made in time for the execution of the instructions.

Allowable Subject Matter

9. Claims 4-7,9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tran (patent No. 6,253,316) disclosed three-state branch history using one bit in a branch prediction mechanism (e.g., see abstract).

Hammond (patent No. 5,638,525) disclosed processor capable of executing programs that contain RISC and CISC instructions (e.g., see abstract).

Krishnan (patent No. 6,356,997) disclosed a system emulating branch instruction of different instruction set in a mixed instruction stream in a dual mode system (e.g., see abstract).

Liu (patent No. 6,088,793) disclosed a system for branch execution on a multiple instruction-set-architecture microprocessor (e.g., see abstract).

Blomgren (patent No. 5,781,750) disclosed dual instruction set architecture CPU with hidden software emulation mode (e.g., see abstract).

Blomgren (patent No. 5,608,886) disclosed block based branch prediction using target finder array storing target sub-addresses (e.g., see abstract).

Asghar (patent 5,794,068) disclosed CPU with DSP having function preprocessor that converts instruction sequences intended to perform DSP function into DSP function identifier (e.g., see abstract).

Bartkowiak (patent No. 5,930,490) disclosed microprocessor configured to switch instruction sets upon detection of a plurality of consecutive instructions (e.g., see abstract).

Poplingher (patent No. 6,021,489) disclosed a system with sharing a branch prediction unit in a microprocessor implementing a two instruction set architecture.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

Art Unit: 2183

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC



Eddie Chan